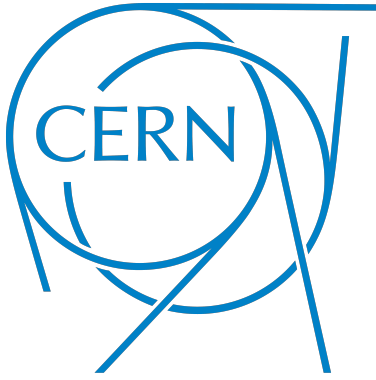




VeloPix Data Visualisation and Read-out Control

LHCb Group

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1 Introduction

1.1 Upgrade of Velo detector

The LHCb (Large Hadron Collider beauty) experiment is one of the four main detectors present in the LHC ring at CERN. During Long Shut-down 2 (LS2) LHCb will undergo a major upgrade, which aims to replace the 1MHz hardware trigger with a software based trigger-less system with a read-out of 40MHz.

For the change in the read-out rate all front-end electronics (FE) need to be replaced. LHCb took this opportunity to redesign its innermost tracking detector the Vertex Locator (VELO). The sensors will change from the current microstrip technology to pixel technology. Their new read-out ASIC is dubbed VeloPix.

In total the Velo upgrade will comprise of 52 sensor modules illustrated in Fig 1, where each module consists of two VELO hybrids, one on the front and on the back side of the module. A hybrid is made up of two tiles, each tile containing three VeloPix ASICs, where each ASIC consists of a 256×256 pixel array, with a pixel size of $55 \times 55 \mu m^2$.

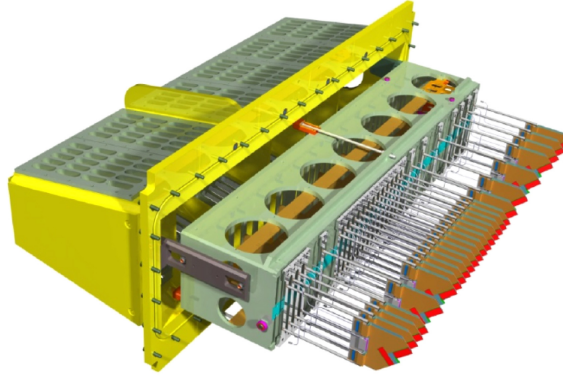


Figure 1: Representation of one detector half of the upgraded Velo. The new pixel sensors are depicted in red.

1.2 Experimental Setup

Currently the system is in its initial testing phase to prepare for manufacturing and assembly. As depicted in Fig 2, the setup devised consists of three main components, as a working framework for development, testing and quality control.

- "MiniDAQ" read-out system
- Opto & Power Board (OPB)
- Front-end Electronics
- GigaBit Transceiver chip (GBTx)

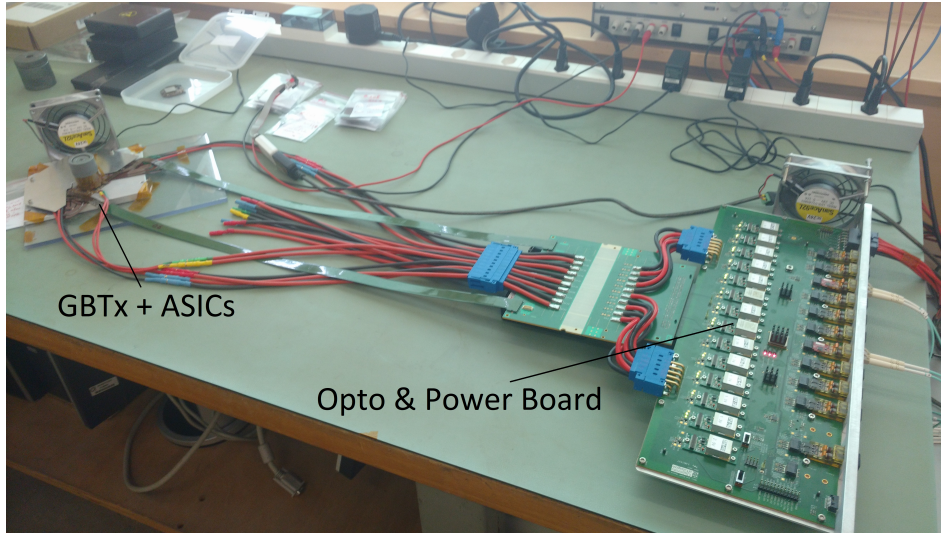


Figure 2: Experimental setup representing the electrical components of a new module, used to develop the data acquisition.

The MiniDAQ consists of an Arria 10 Altera FPGA chip, and a GBT server, where the latter is responsible for the communication between the user and the firmware on the FPGA. The MiniDAQ communicates to the experimental setup through optical fibre links. In the test setup they are less than one meter in length, but will span more than 100m for the final detector.

The Opto & Power Board (OPB) converts the electrical data and control signals from the hybrid module to optical data over the fibre links to the MiniDAQ, and vice-versa. Furthermore, it provides the multiple voltage rails supplied to the GBTx, VeloPix ASICs and the optical links transceivers. It is configured and monitored using a GBTx.

The front-end electronics consist of the VeloPix ASICs, and a second GBTx used to configure the ASICs.

1.3 Testing Sequence

To verify the read-out chain, a number of steps are required which will be further discussed in later sections.

- Firmware Verification
- OPB Configuration
- ASIC Communication
- Timing & Fast Control (TFC)
- Equalisation Process

The firmware is being developed by the LHCb online group, but there is a VELO specific part which requires to be tested. This includes the algorithm to read from and write to the VeloPix ASICs.

The OPB generates the necessary voltage rails for the module to function, while tracking the individual outputs for correct operation. An additional monitor is provided on the input voltage supplied, which currently is set to 6V. Furthermore, the OPB controls the configuration of the laser drivers for the optical links.

Afterwards, communication with the VeloPix ASICs is verified through the GBTx by completing a set of basic Read and Write operations to these ASICs.¹

The TFC protocol provides a set of commands to synchronise the FE, between the different sub-detectors and DAQ system, for further detail refer to [1]. It should be tested that the VeloPix responds correctly to these commands.

The first non-trivial test of the VeloPix's performance is the 'Equalisation'. It refers to the procedure of aligning all pixel's noise responses through the 4-bit fine tuning offset parameter that each pixel has, as illustrated in Fig 3. The alignment is done with respect to the mean noise response of the majority of the pixels. By tuning the offset parameter the individual response can be adjusted to match the desired noise spectrum. Additionally, those pixels whose noise response can not be adjusted to the desired behaviour are masked to reduce the noise output of the chip. Specification of the procedure and respective outputs are discussed in Section 2.1.

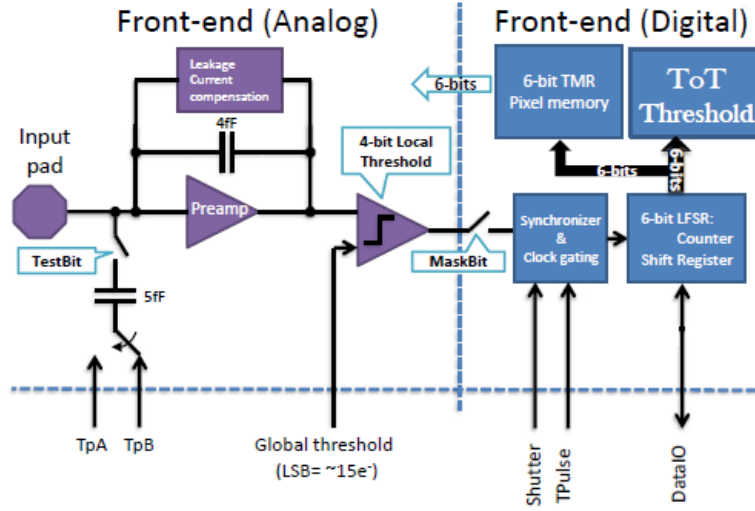


Figure 3: VeloPix pixel schematic with 4-bit offset and mask bit

¹An additional set of tests were carried out on a sample batch of GBTx to verify their operation, and label them respectively for future reference.

1.4 Project Aim

The main scope of this project is to visualise the outcome of the equalisation process, which allows the user to identify possible issues with an ASIC and/or the read-out chain. The focal plot representing the different steps taken to obtain the equalised range, additionally an optional test run to verify the equalisation process. The equalisation process also includes the 4-bit fine tuning offset, mask and noise files, which are displayed in a 256x256 pixel array format.

Since the VELO upgrade is currently shifting from research and development to manufacturing and assembly, it was necessary to develop a number of user-interfaces which allows the testing and verification of the individual components of the read-out chain. These user-interfaces will be used throughout the assembly process to monitor the electrical functions of the modules as they are build and installed.

2 Data Visualisation

2.1 Equalisation

As previously stated, the equalisation process aligns each pixel noise response via the 4-bit fine tuning offset parameter such that the majority of pixels have a common response. Pixels which cannot be equalised are masked such that their output does not skew the results. Hence, the three main components that constitute the equalisation, are:

- Computation of a uniform threshold per ASIC.
- Computation of the 4-bit fine offset parameter per pixel.
- The mask bit per pixel.

The process to obtain the noise response from an ASIC consists of applying a DAC threshold sweep between a minimum and maximum threshold value where the 4-bit fine tuning offset parameter of each pixel is initially set to 0, and a second repetition with the offset set to 15. The combination of both the 0 (red) and 15 (blue) noise spectra see Fig 4 is used to compute a target threshold for the 4-bit offset, which shall provide a uniform response per ASIC.

Ideally, the resultant output (black in Fig 4) referred to as “Predicted” should converge to a straight line at one specific DAC threshold, however this is not the case due to the fact that the fine tuning parameter has only a 4-bit precision which limits the minimum range that the offset can be adjusted by. Additionally, a second cause for the range of equalisation is due that the two noise spectra have an overlapping region.

Furthermore, an additional DAC threshold sweep, which uses the parameters generated from the equalisation process, can be executed to verify the prediction depicted by the green plot.

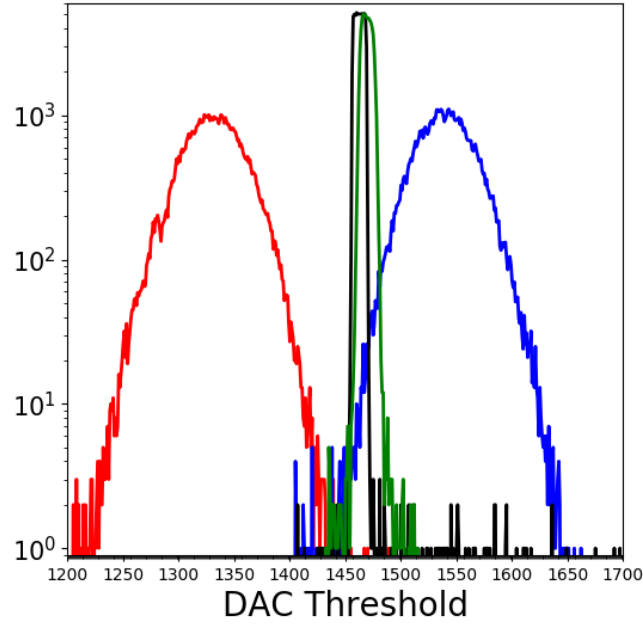


Figure 4: Outcome of the equalisation process; Red is the noise response with the 4-bit offset tuning parameter set 0, and the Blue with the parameter set to 15. Black refers to the predicted result from the equalisation and Green is the Test results after equalisation.

2.1.1 Additional Parameters

Figure 5 is the generated mask file which disables the individual pixel within the ASIC whose noise spectrum cannot be equalised. The red dots relate to the masked pixels, moreover one can identify possible issues in an ASIC where in this case column 169 was entirely masked inferring a hardware failure in the chip.

Figures 6 & 7 refer to the ASIC pixel grid noise spectrum and 4-bit offset setting, respectively. To further distinguish the validity of each parameter, the bit-mask per pixel was inserted as an overlay to identify masked pixels. Additional attributes were obtained through the histogram plot of the noise width, from which the mean and standard deviation were calculated.

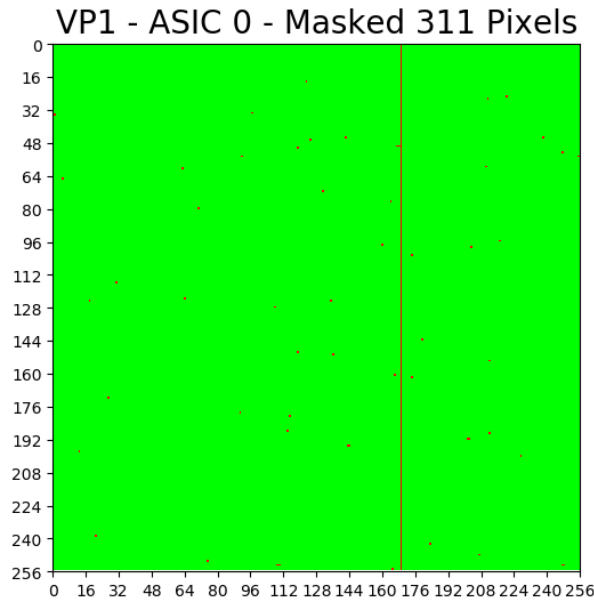


Figure 5: Bit Mask plot

VP1 - ASIC 0

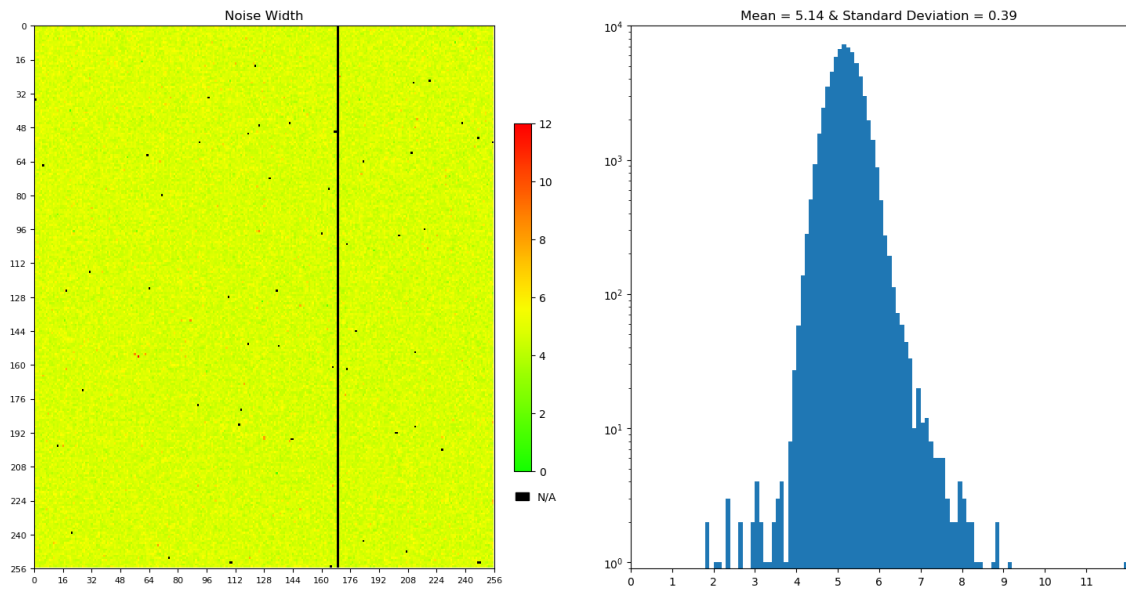


Figure 6: ASIC Noise-Spectrum grid and histogram

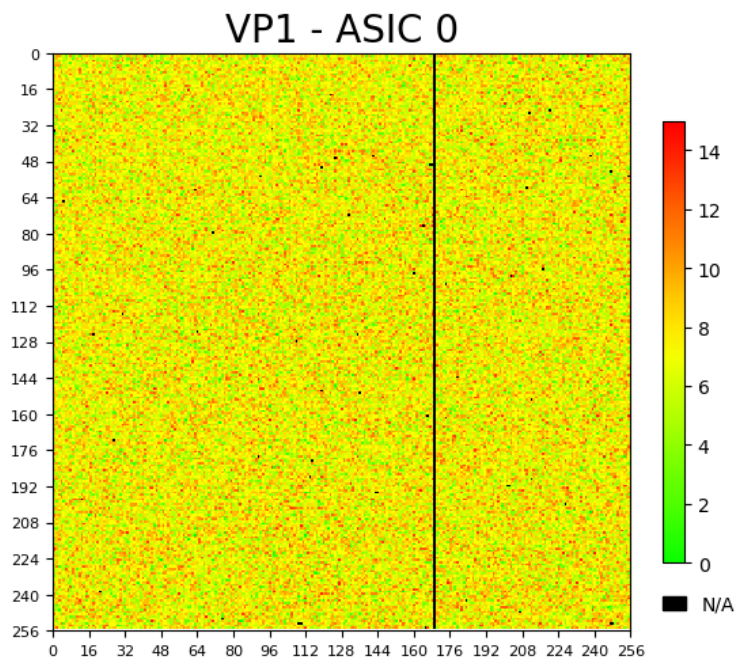


Figure 7: ASIC 4-bit Offset setting

2.2 ECS Data

The slow control (ECS) interface provides read back capability to every register in the VeloPix. Using this interface, it is possible to take data, although at a much reduced rate. This nonetheless allows to test the read-out chain using cosmic muons (Fig 8a) or a radioactive source (Fig 8b)

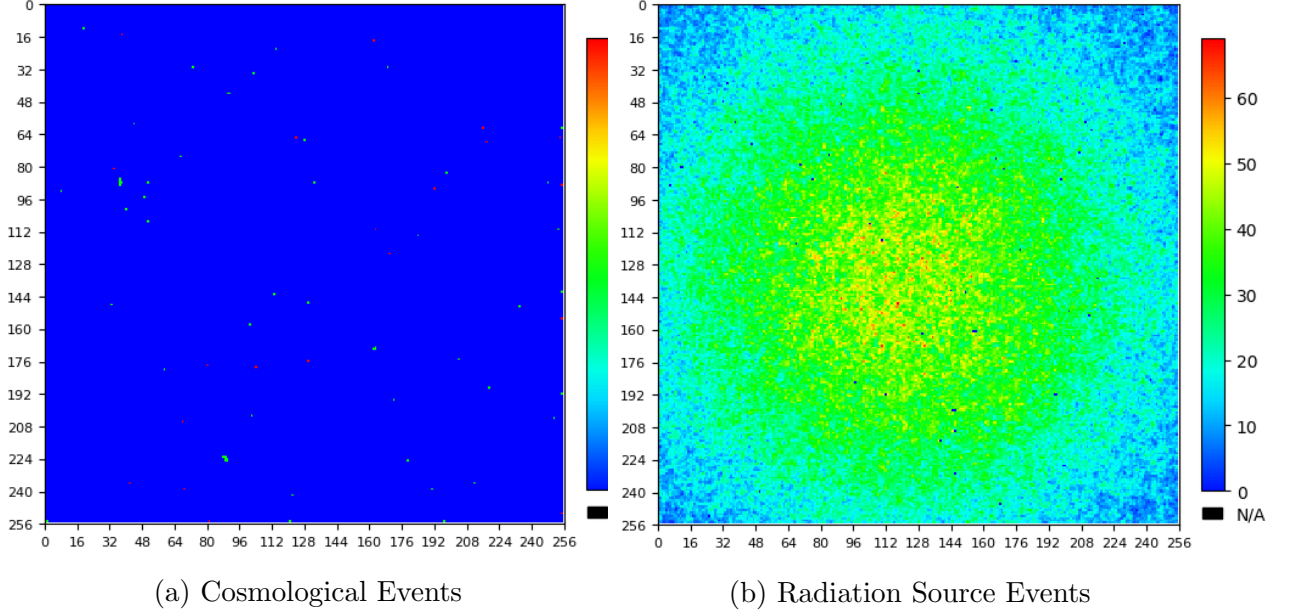


Figure 8: Two types of event measurements using ECS data path.

The experiment was conducted by setting the respective ASIC threshold value equal to the equalisation value obtained from the aforementioned process and adding a 100 to ensure that the triggers registered are cosmological events and not affected by pixel noise. This was due to the fact that for background hits, there were a number of pixels which saturated, as indicated in Figure 8a by the red dots.

For a radioactive source, the results produced are beneficial in the identification of erroneous pixel behaviour or pixels not bump-bonded successfully to the sensor by identifying regions in an ASIC whose output number of events is lower than the neighbouring pixels. In Figure 8b, a number of dots are colder within the central portion of the radioactive source, due that the bits were masked.

3 Control and DAQ Interfaces

Data monitoring of device registers, data logging, and development of user interfaces were implemented through WinCC OA, which is a tool used to develop SCADA based applications. Moreover, because the different components of a module are developed and tested off-site by associate groups, requires that the programs in question provide a user-friendly application to monitor and debug individual parameters.

The following are panels which were either created or modified during the project, for further debugging.

1. Voltage Monitor - Tracks input voltages to the OPB.
2. TFC Signals - Monitors a number of registers counting the received TFC commands per ASIC.
3. Equalisation Scan - Provides control and reviewing over the equalisation process.
4. Register Control - Firmware debugging panel.

3.1 Voltage Monitor

This panel serves as a diagnostic monitor for the input voltage to the OPB board.

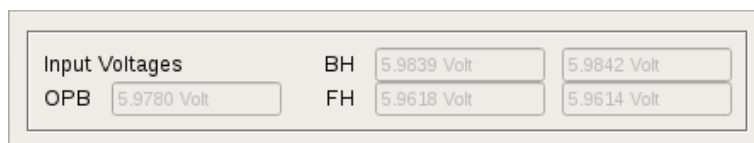


Figure 9: DC-DC Power Monitor

The OPB DAQ application, uses this simple voltage monitor within one of its steps to verify operation of the system, presented in Figure 10. Additionally, this panel monitors the MiniDAQ server along with the multiple voltage regulators in use by the sensor module and the configuration settings of the optical drivers. Hence, through this application the initial configuration of both the MiniDAQ and OPB can be set for normal operation of the system, and further debugging.

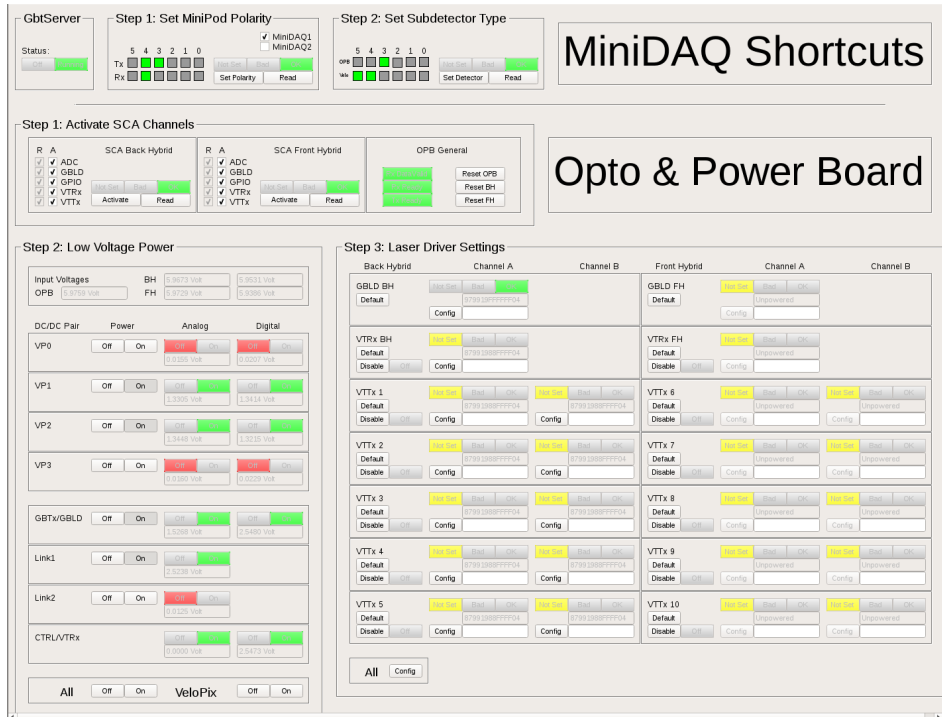


Figure 10: OPB panel with default settings for the Back Hybrid configuration.

3.2 TFC Signals

The panel presented in Figure 11, provides watch over a number of timing and fast control (TFC).

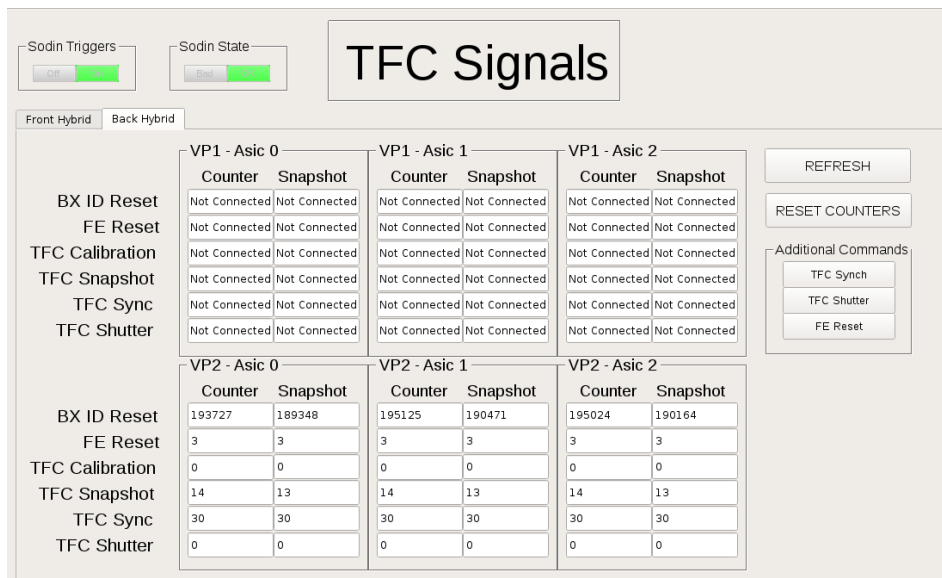


Figure 11: TFC Signal monitor system

3.3 Equalisation Panel

After the initial setup of a module, each individual ASIC is to be equalised as described in 2.1. The user can initiate an equalisation run or provide a directory which contains pre-computed equalised data from which Figures 4 through 7 can be reviewed.

Figure 12 illustrates the available options, and displays the predicted result from the equalisation process.

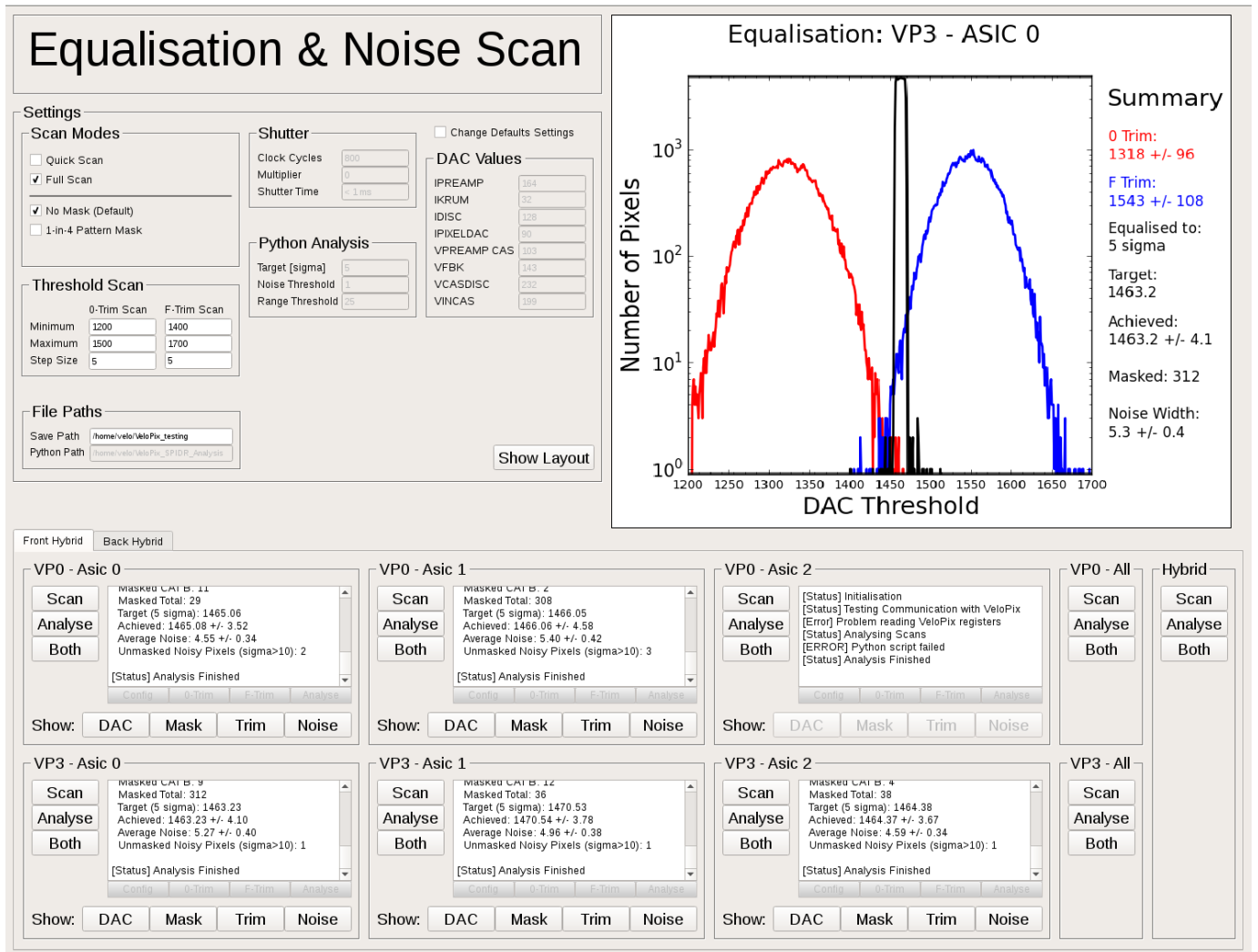


Figure 12: Equalisation Control panel

3.4 Register Control

Figure 13, shows a panel which provides an additional verification step of the FPGA firmware. A step-by-step process is listed:

1. The user must specify the address in the firmware for the Velo-specific registers. These are grouped per ASIC, which therefore also must be specified.
2. Set the global parts of the firmware into Velo-specific mode.

Commands for the VeloPix ASICs are constructed word-by-word individual FIFO registers before being shipped off in one single package to the chip. Communication to and from the VeloPix is identified by a fixed header: 0xE8. Likewise, responses from the ASICs are collected in a FIFO before being processed by the firmware.

3. Send a flush operation, which writes the 6-bit value 0x3F to read and write the FIFOs. Where the value 0x3F represents the six ASICs present in the hybrid, which reset both FIFOs. After a read operation, a result of 0x0003F03F indicates successful execution.
4. Additionally, an automatic routine sets a flush operation, write the header command 0xE8 which is an identifier for the system that the following transmission is intended for the ASICs. Since the experimental setup was in loop-back and assuming that the operation is done for ASIC 0, the data transmitted is 0x3E, after the command is sent the firmware receivers will identify the header 0xE8 and store the data, which for a successful write operation the receiver should have the value 0x3E.

VeloPix FIFOs

Step 1: Specify Register

Host PC: lhcb-asus01

Control: 0x 760 Invalid Valid

Asic: ☒ Separate Go-Velo Regs

Step 2: Set Subdetector

Set Read Set

Step 3: Test Flushing FIFOs

Flush Read

Step 4: Test Sending Header

Send E8

Output

```
[CONTROL REG] 0003F03F
[Action] Flushing Tx FIFO 00504640
[Action] Flushing Rx FIFO 00504644
[CONTROL REG] 0003F03F
[Action] Filling Tx FIFO 00504600
[CONTROL REG] 0003E03F
[Action] Sending Go Velo 00504618
[CONTROL REG] 0003F03E
```

Clear Bad OK

Figure 13: FIFO test panel

References

- [1] LHCb Collaboration *LHCb VELO Upgrade Technical Design Report*, Rep. CERN-LHCC-2013-021. LHCb-TDR-013, Nov, 2013.